

Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application.

1. (Current Amended) A latch circuit, comprising:

a bistable pair of transistors connected between a reset switch and a first supply voltage, and having a first port for receiving a first current signal and producing a first output voltage, and a second port for receiving a second current signal and producing a second output voltage; and

a vertical latch connected between said first supply voltage and a second supply voltage, and connected to said first port, said vertical latch having a transistor connected to said ~~first supply voltage but isolated from said second supply voltage~~, wherein said transistor is configured to amplify a change in said first output voltage in response to said first current signal received first port so that, when said transistor is turned on, a current flows from said second supply voltage through said transistor to said first port.

2. (Original) The latch circuit of claim 1, wherein said transistor is a MOSFET.

3. (Original) The latch circuit of claim 1, wherein said reset switch is a microelectromechanical reset switch.

4. (Previously Presented) The latch circuit of claim 1, wherein said vertical latch is for decreasing the time necessary for said first port to reach a steady state voltage in response to said first current signal received.

5. (Original) The latch circuit of claim 1, further comprising a vertical latch reset switch connected to said vertical latch.

6. (Original) The latch circuit of claim 1, further comprising a second vertical latch connected between said first supply voltage and said second supply voltage, and connected to said second port.

7. (Currently Amended) A latch circuit, comprising:

a bistable pair of transistors connected between a reset switch and a first supply voltage, and having a first port for receiving a first current signal and producing a first output voltage, and a second port for receiving a second current signal and producing a second output voltage; and

a vertical latch connected between said first supply voltage and a second supply voltage, and connected to said first port;

wherein said vertical latch comprises:

a first current mirror pair connected at a node to said ~~bistable pair of transistors~~ first port; and

a second current mirror pair connected at said node to said ~~first current mirror pair port~~.

8. (Original) The latch circuit of claim 7, wherein a current gain of said first current mirror pair is less than one.
9. (Original) The latch circuit of claim 7, wherein said reset switch is a microelectromechanical reset switch.
10. (Previously Presented) The latch circuit of claim 7, wherein said vertical latch is for decreasing the time necessary for said first port to reach a steady state voltage in response to said first current signal received.
11. (Original) The latch circuit of claim 7, further comprising a vertical latch reset switch connected to said vertical latch.
12. (Original) The latch circuit of claim 7, further comprising a second vertical latch connected between said first supply voltage and said second supply voltage, and connected to said second port.
13. (Currently Amended) A reset circuit for a latch circuit having a bistable pair of transistors ~~connected to a supply voltage~~, the reset circuit comprising:
 - a first transistor connected to ~~the~~ a supply voltage at a first ~~terminal of said first transistor node~~;

a second transistor connected ~~between a second terminal of~~ to said first transistor at a second node and to a first port of the latch circuit, wherein a gate terminal of said second transistor is connected to a drain terminal of said second transistor at said first port; and

a third transistor connected ~~between said second terminal of~~ to said first transistor at said second node and to a second port of the latch circuit, wherein a gate terminal of said third transistor is connected to a drain terminal of said third transistor at said second port;

wherein transistors of said latch circuit, said first transistor, said second transistor, and said third transistor are all characterized by a common channel type, said common channel type being one of a p-channel type and a n-channel type.

14. (Original) The reset circuit of claim 13, wherein at least one of said first transistor, said second transistor, and said third transistor is a MOSFET.

15. (Currently Amended) An analog-to-digital converter, comprising:

a comparator having a first input for receiving an analog signal and a second input for receiving a reference signal, said comparator for producing a digital signal;

wherein said comparator comprises a latch circuit having a bistable pair of transistors coupled between a reset circuit and a first supply voltage, and a vertical latch coupled between said first supply voltage and a second supply voltage and coupled to said bistable pair of transistors at a node coupled to said reset circuit, said vertical latch having a first transistor and a second transistor, said first transistor being of a first

channel type, said second transistor being of a second channel type, said first channel type being one of a p-channel type and a n-channel type, said second channel type being different from said first channel type, and said first transistor is coupled to said bistable pair of transistors at said node so that, when said first transistor is turned on, a current flows from said second supply voltage through said first transistor to said node.

16. (Original) The analog-to-digital converter of claim 15, wherein at least one of said first transistor and said second transistor is a MOSFET.

17. (Currently Amended) A In a latch circuit, a method for decreasing the time in which a first latch circuit port receiving a current signal greater than a bias current reaches a first steady state voltage, comprising the steps of:

(1) amplifying the current signal greater than the bias ~~current~~ while maintaining a current signal less than the bias current received at a second latch circuit port; current; and

(2) applying said amplified current signal to the first latch circuit port receiving the current signal greater than the bias current port;

wherein the first steady state voltage is a high voltage, a second steady state voltage of a second latch circuit port receiving a current signal less than the bias current is a low voltage, and the first latch circuit port and the second latch circuit port are at a middle voltage when a reset circuit couples the first latch circuit port to the second latch circuit port.

18. (Currently Amended) In a latch circuit having a bistable pair and a vertical latch, ~~wherein the bistable pair has a first transistor and a second transistor configured so that a first type terminal of the first transistor is connected to a second type terminal of the second transistor at a first port, a first type terminal of the second transistor is connected to a second type terminal of the first transistor at a second port, and a third type terminal of the first transistor and a third type terminal of the second transistor are connected together, and wherein the vertical latch has a third transistor and a fourth transistor configured so that a second type terminal of the third transistor is connected to a second type terminal of the second transistor and a first type terminal of the fourth transistor, a third type terminal of the third transistor is connected to a first supply voltage, a third type terminal of the fourth transistor is connected to a second supply voltage, and a second type terminal of the fourth transistor is connected to a first type terminal of the third transistor,~~ a method for reducing the power consumed by the latch circuit, comprising the steps of:

(1) resetting the bistable pair and the vertical latch; and

(2) holding the a fourth transistor OFF during said ~~resetting~~ resetting;

wherein the bistable pair has a first transistor and a second transistor configured so that a first type terminal of the first transistor is connected to a second type terminal of the second transistor at a first port, the first type terminal of the second transistor is connected to the second type terminal of the first transistor at a second port, and a third type terminal of the first transistor and the third type terminal of the second transistor are connected together, and wherein the vertical latch has a third transistor and the fourth transistor configured so that the second type terminal of the third transistor is connected

at a first node to the second type terminal of the second transistor and to the first type terminal of the fourth transistor, the third type terminal of the third transistor is connected to a first supply voltage, the third type terminal of the fourth transistor is connected to a second supply voltage, and the second type terminal of the fourth transistor is connected at a second node to the first type terminal of the third transistor.

19. (Currently Amended) The In a latch circuit having a bistable pair and a vertical latch, a method of claim 18, wherein step (2) comprises for reducing the power consumed by the latch circuit, comprising the step steps of:

(1) resetting the bistable pair and the vertical latch; and
(3) (2) holding the a third transistor OFF during said resetting. resetting;
wherein the bistable pair has a first transistor and a second transistor configured so that a first type terminal of the first transistor is connected to a second type terminal of the second transistor at a first port, the first type terminal of the second transistor is connected to the second type terminal of the first transistor at a second port, and a third type terminal of the first transistor and the third type terminal of the second transistor are connected together, and wherein the vertical latch has the third transistor and a fourth transistor configured so that the second type terminal of the third transistor is connected at a first node to the second type terminal of the second transistor and to the first type terminal of the fourth transistor, the third type terminal of the third transistor is connected to a first supply voltage, the third type terminal of the fourth transistor is connected to a second supply voltage, and the second type terminal of the fourth transistor is connected at a second node to the first type terminal of the third transistor.

20. (Currently Amended) ~~The In a latch circuit having a bistable pair and a vertical latch, a method of claim 18, wherein step (2) comprises for reducing the power consumed by the latch circuit, comprising the step steps of:~~

- (1) resetting the bistable pair and the vertical latch; and
- (4) (2) after said resetting, holding the a fourth transistor OFF when the a second transistor changes state from ON to OFF. OFF;

wherein the bistable pair has a first transistor and the second transistor configured so that a first type terminal of the first transistor is connected to a second type terminal of the second transistor at a first port, the first type terminal of the second transistor is connected to the second type terminal of the first transistor at a second port, and a third type terminal of the first transistor and the third type terminal of the second transistor are connected together, and wherein the vertical latch has a third transistor and the fourth transistor configured so that the second type terminal of the third transistor is connected at a first node to the second type terminal of the second transistor and to the first type terminal of the fourth transistor, the third type terminal of the third transistor is connected to a first supply voltage, the third type terminal of the fourth transistor is connected to a second supply voltage, and the second type terminal of the fourth transistor is connected at a second node to the first type terminal of the third transistor.